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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,036	03/07/2001	Maged M. Michael	YO919990425	4574

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Robert P. Tassinari, Jr.
Intellectual Property Law Dept.
IBM Corporation
P.O. Box 218
Yorktown Heights, NY 10598

EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	8

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,036	MICHAEL ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4, 7-15, 17-20,22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-14,20 and 25* is/are allowed.

6)☒ Claim(s) *1-4,7,15,17-19,22,24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed July 21, 2003 in response to PTO Office Action mailed April 17, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims have been presented for examination in this application. In response to the last Office Action, claims 1, 8, 15, 19, 20 and 22 have been amended. Claims 5, 6, 16, 21 and 23 have been canceled. No claims have been added. As a result, claims 1-4, 7-15, 17-20, 22 and 24-26 are now pending in this application.

3. The objection to the drawings has been withdrawn due to the amendment filed July 21, 2003.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 7, 19, 22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al. (US5,864,671) and Smith et al. (US6,055,610).

As per claim 1, Hagersten discloses a system for maintaining consistent cached copies of memory in a multi-node computing system having a main memory comprising: at least one memory directory having memory directory entries mapping the main memory [*each directory entry 602 in directory 601 corresponds to a unique memory block;* col. 7, lines 40-43], one or more of the memory directory entries including state information for a corresponding line of main memory [*each directory entry 602 includes a field for storing the directory states of the corresponding memory blocks;* col. 7, lines 44-46]; at least one directory cache for storing directory cache lines corresponding to subset of the memory directory entries [*directory cache 604 contains directory cache entries 603 representing a subset of directory entries 602;* col. 7, lines 51-54]; and means for using the state information to allocate memory directory entries to the directory cache [*request is serviced based on whether a first node contains a valid copy of the memory block;* col. 9, lines 2-5].

However, Hagersten does not specifically teach said at least one directory cache disposed within the functionality of a corresponding coherence controller; and at least one single-bit sharing history indicator corresponding to each of at least one memory

directory, said at least one single-bit sharing history indicator indicating a first value or a second value, wherein the first value indicates that only one node maintains a cached copy of the corresponding line of main memory and the second value indicates that more than one node maintains a cached copy of the corresponding line of main memory as recited in the claim.

Smith discloses a at least one directory cache disposed within the functionality of a corresponding coherence controller (Fig. 1, *directory cache FD and coherency controller CC*); and at least one single-bit sharing history indicator corresponding to each of at least one memory directory (*sharing bit distinguishes cases in which data is cached by at most one cell and data that is cache by two or more cells*; col. 9, lines 15-20) for improving computer performance by reducing access time. Since the technology for implementing a directory cache disposed within the functionality of a corresponding coherence controller and a single-bit sharing history indicator was well known, and since a directory cache disposed within the functionality of a corresponding coherence controller and a single-bit sharing history indicator improves computer performance by reducing access time, an artisan would have been motivated to implement these features in the system of Hagersten. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a directory cache disposed within the functionality of a corresponding coherence controller and a single-bit sharing history indicator, because these features were well known to improve computer performance by reducing access time as taught by Smith.

As per claim 2, Hagersten discloses the use for using the state information comprises determining sharing behavior of a memory line corresponding to the state information [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

As per claim 7, Hagersten discloses the subset of memory directory entries corresponds to a set of most frequently used memory directory entries [*directory cache caches commonly used memory blocks;* col. 18, lines 1-3].

As per claims 19 and 22, Hagersten discloses the claimed invention as detailed above per claim 1 above. Hagersten further discloses a processor cache [*memory cache 702*, Fig. 7]; receiving a signal at the directory cache in one node of the system indicative of a coherence request for a cached memory line from one of the other nodes of the system [*receiving a memory access request from a first node;* col. 8, lines 61-63]; performing a memory directory lookup to determine the location of the directory entry of the cached memory [*consulting the directory cache to determine which node possesses a copy of the memory block;* col. 9, lines 2-5]; storing information describing the sharing behavior of the cached memory line [*storing validity and state information in directory cache;* col. 17, lines 53-62].

However, Hagersten does not specifically teach at least one single-bit sharing history indicator as recited in the claims.

Smith discloses a single-bit sharing history indicator (*sharing bit distinguishes cases in which data is cached by at most one cell and data that is cache by two or more cells*; col. 9, lines 15-20) for improving computer performance by reducing access time. Since the technology for implementing a single-bit sharing history indicator was well known, and since a single-bit sharing history indicator improves computer performance by reducing access time, an artisan would have been motivated to implement that feature in the system of Hagersten. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a single-bit sharing history indicator, because it was well known to improve computer performance by reducing access time as taught by Smith.

As per claims 24 and 26, the combination of Hagersten and Smith discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Smith does not particularly disclose a program storage device, readable by a machine, tangibly embodying a program of instructions executable by the machine to perform the method steps of claims 19 and 22. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, CD-ROM, etc.) carrying computer executable instructions for implementing a method, because it would facilitate the transportation and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a CD-ROM from which Windows can be installed onto other systems, which is a lot easier than running a long cable or hand typing the software into another system. The examiner takes Official Notice of this

teaching. Therefore, it would have been obvious to put Hagersten and Smith's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Hagersten and Smith's program on other systems.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Smith et al. (US6,055,610) and Young et al (US5,860,120).

As per claim 3, Hagersten and Smith disclose the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Smith does not specifically teach the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines as recited in the claim.

Young discloses the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines [*a three bit entry indicates whether the line is cached, exclusive or shared;* col. 4, lines 34-40].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Smith and Young before him at the time the invention was made, to modify the system of Hagersten and Smith to include the state information includes at least one bit in each of the memory directory entries, said at least one bit

indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

As per claim 4, Hagersten and Smith disclose the claimed invention as detailed above in the previous paragraphs. However, the combination of Hagersten and Smith does not specifically teach the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry as recited in the claim.

Young discloses the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry [*status table identifies which processors have which lines of memory in their associated caches;* col. 4, lines 20-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Smith and Young before him at the time the invention was made, to modify the system of Hagersten and Smith to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

7. Claims 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US5,864,671) and Smith et al. (US6,055,610) and Young et al (US5,860,120).

As per claim 15, Hagersten discloses a system for maintaining consistent cached copies of memory in a multi-node computing system having a main memory comprising: at least one memory directory having memory directory entries mapping the main

memory [*each directory entry 602 in directory 601 corresponds to a unique memory block;* col. 7, lines 40-43].

However, Hagersten does not specifically teach at least one directory cache disposed within the functionality of a corresponding coherence controller; the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry as recited in the claim.

Smith discloses at least one directory cache disposed within the functionality of a corresponding coherence controller (Fig. 1, *directory cache FD and coherency controller CC*); for improving computer performance by reducing access time. Since the technology for implementing a directory cache disposed within the functionality of a corresponding coherence controller was well known, and since a directory cache disposed within the functionality of a corresponding coherence controller improves computer performance by reducing access time, an artisan would have been motivated to implement that feature in the system of Hagersten. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a directory cache disposed within the functionality of a corresponding coherence controller, because these features were well known to improve computer performance by reducing access time as taught by Smith.

Young discloses the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an

associated data cache that contains a copy of a memory line corresponding to such memory directory entry [*status table identifies which processors have which lines of memory in their associated caches;* col. 4, lines 20-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Young before him at the time the invention was made, to modify the system of Hagersten to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

As per claim 18, Hagersten discloses the claimed invention as detailed above in the previous paragraphs. However, Hagersten does not specifically teach the state information includes at least one bit in each of the memory directory entries, said at

least one bit indicating sharing behavior of its corresponding memory lines as recited in the claim.

Young discloses the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines [*a three bit entry indicates whether the line is cached exclusive or shared;* col. 4, lines 34-40].

It would have been obvious to one of ordinary skill in the art, having the teachings of Hagersten and Young before him at the time the invention was made, to modify the system of Hagersten to include the state information includes at least one bit in each of the memory directory entries, said at least one bit indicating sharing behavior of its corresponding memory lines and the state information in a memory directory entry includes data indicating which one or more nodes in the multi-node computing system have an associated data cache that contains a copy of a memory line corresponding to such memory directory entry because it would have provided an improved directory-based cache coherency memory system by reducing memory overhead requirement for the storage of memory state information [col. 1, lines 46-47, 59-60] and by reducing the amount of work that must be performed until a processor needs data that resides in a cache that cannot be accessed through snooping [col. 4, lines 25-28] as taught by Young.

As per claim 17, Hagersten discloses the use for using the state information comprises determining sharing behavior of a memory line corresponding to the state

information [*request from another node can be advantageously serviced when the home node has a shared copy;* col. 15, line 57-67].

Allowable Subject Matter

8. Claims 8-14, 20 and 25 are allowed over the prior art of record.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest "means for using state information to select a directory cache line with the least memory directory entries for the corresponding line of main memory cached in two or more nodes and evict the directory cache lines in the directory cache" in combination with the other elements set forth in claims 8 and 20.

Therefore, dependent claims 9-14 and 25 are allowable as being dependent upon independent 8 and 20 and having additional allowable features therein.

Response to Arguments

10. Applicant's arguments with respect to claims 1-4, 7-15, 17-20, 22 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre M. Vital
Art Unit 2188
April 5, 2004